

Parallel Absolute Output

The two most common types of absolute outputs are the Gray Code and the Natural Binary. Resolution for absolute encoders is expressed in “bits” where each successive bit increases the resolution by a factor of two. For example, 10 bits = $2^{10} = 1024$ counts per revolution.

Natural binary code (Figure 1) is constructed so that the code counts up using the natural sequence of binary counting, i.e. 000, 001, 010, 011, 100 . . . etc. The drawback to using this code sequence is that at several count positions the code will have transitions on multiple bits simultaneously. Due to the normal variations caused by gate delays, line impedances, etc. the actual transitions will not occur simultaneously. Reading data during one of these times could result in an erroneous reading. This can be overcome by taking multiple readings.

Gray code (Figure 2), by contrast, is designed to avoid the multiple transition problem entirely. It is specifically constructed so that only one bit will transition at a time. This ensures that state changes are much less ambiguous to the controller and is generally considered to be a more robust type of absolute code.

Regardless of the code type, one of the characteristics of absolute encoders is that they can readily be used for any resolution up to and including their maximum resolution. For example, a 12 bit encoder can be used at only 8 bits by ignoring (or disconnecting) the four lowest significant bits (LSB). This enables an installation that uses multiple absolute encoders to use the same encoder throughout with each controller using only the bits that it needs.

Figure 1 Natural Binary

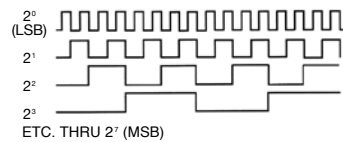
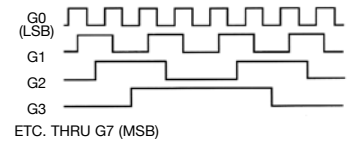


Figure 2 Gray Code



Ordering 8-Bit Absolutes

For years, we produced encoders with a maximum resolution of 8 bits. Lots of those old 8 bit encoders are still around. We update them to newer 12 bit designs on a case-by-case basis. If you have an 8 bit encoder, here is how that model number was constructed: **Direction of Rotation, Count, Code** and **Latch** designators were inserted between **Shaft Seal Configuration** and **Voltage/Output** as shown below. To specify an equivalent encoder based on the 12 bit design, please call our Applications Specialists at **800-ENCODER** (800-362-6337) or check our website at www.beiied.com.

Direction of Rotation: CCW or CW

Count: 8

Code: GC= Gray Code or NB= Natural Binary

Latch: L= Latch or Blank=None

Output Terminations: EM20=MS3102R20-29P or ED25=DB25P; SM18 = MS3102R18-1P; C18 = Cable, with length specified in inches. Specify ED25 for Line Driver Outputs.

Example: H25E-F1-SS-CCW-8GC-28V/V-EM20

(one possible encoder configuration with the 8-Bit Absolute Option.)

Serial Synchronous Interface (SSI)

SSI output provides effective synchronization in a closed-loop control system. A clock pulse train from a controller is used to clock out sensor data: one bit of position data is transmitted to the controller per one clock pulse received by the sensor. The use of a differential driver permits reliable transmission of data over long distances in environments that may be electrically noisy. The encoder utilizes a clock signal, provided by the user interface, to time the data transmission. Receiving electronics must include an appropriate receiver as well as line terminating resistors.

Features

- Synchronous transmission
- Transmission lengths to 1000 feet
- Accepts clock rates from 100 KHz to 1.8 MHz

Data Transmission Sequence

1. Output driver of the encoder is a MAX 491 transceiver in transmit mode. The recommended receiver is a MAX 491 transceiver in receive mode.
2. Controller provides a series of pulses (or differential pulse pairs) on the CLOCK input lines.
3. On the first HIGH-to-LOW CLOCK transition, the encoder latches its data at the current position and prepares to transmit.
4. Controller reads data on the falling edge of the next 15 clock cycles.
5. The first bit is a START bit and is always HIGH.
6. Next comes 13 data bits beginning with the most significant bit (MSB) and ending with the parity bit. On 12 bit encoders, bit 13 is LOW. When parity is not ordered, parity is LOW.
7. After the DATA bits, the DATA line goes LOW and remains LOW for a minimum of 20 microseconds between the end of the DATA bits and the beginning of the next CLOCK series.

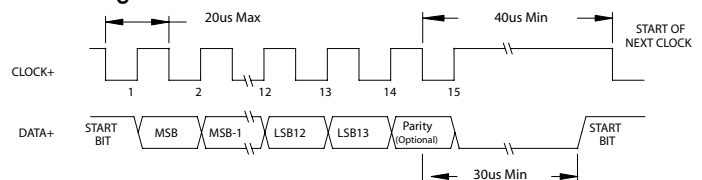
Interfacing Long Data Lines

Cable impedance can create a transmission delay, in effect, shifting the phase relationship between the clock pulse and the data. If this phase shift exceeds 180°, then the wrong bit position will be sampled by the receiver. As a result, the maximum allowable clock frequency is a function of the cable length. For 24 AWG, stranded, 3 pair cable (BEI part number 37048-003 or equivalent) the group delay is 1.36ns/ft. The table below shows the maximum transmission rate allowable as a function of cable length to ensure a phase shift of less than 90°.

CLOCK, Maximum (kHz) = 92,000 / Cable Length (ft)CW

Cable Length (ft)	50	100	200	300	500	1000
Max Freq (kHz)	1800	900	500	300	200	100

SSI Timing



Ordering SSI

HOW TO SPECIFY SSI OUTPUT IN THE ENCODER MODEL NUMBER:

Use the designation, S3 between the **Code Format** designation and the **Connector** designation.

Example: H25D-SS-12GC-S3-CW-SM18



Single Turn Absolute Encoder Options

The tables below are reference for pinouts, connections and operation of BEI's single turn absolute encoders. These absolute options are available in a wide range of package styles with a variety of outputs. The applicability table below shows which combinations are currently available. As always, you can call us at **800-350-ASAP (2727)** for immediate applications assistance should you have any questions.

Output Code and Terminations (12 & 13 Bit)								
PARALLEL CODE						TERMINATION TYPE		
	Gray Code		Natural Binary		Binary Coded Decimal	Cable Conn	M14/19	Term Board H38 & H40
	12 Bit	13 Bit	12 Bit	13 Bit				
MSB	G ₁₁	G ₁₂	2 ¹¹	2 ¹²	A ₀	WHT/BLK	A	1
	G ₁₀	G ₁₁	2 ¹⁰	2 ¹¹	B ₀	WHT/BRN	B	2
	G ₉	G ₁₀	2 ⁹	2 ¹⁰	C ₀	WHT/RED	C	3
	G ₈	G ₉	2 ⁸	2 ⁹	D ₀	WHT/ORN	D	4
	G ₇	G ₈	2 ⁷	2 ⁸	A ₁	WHT/YEL	E	5
	G ₆	G ₇	2 ⁶	2 ⁷	B ₁	WHT/GRN	F	6
	G ₅	G ₆	2 ⁵	2 ⁶	C ₁	WHT/BLU	G	7
	G ₄	G ₅	2 ⁴	2 ⁵	D ₁	WHT/VIO	H	8
	G ₃	G ₄	2 ³	2 ⁴	A ₂	WHT/GRY	J	9
	G ₂	G ₃	2 ²	2 ³	B ₂	WHT	K	10
LSB ₁₂	G ₁	G ₂	2 ¹	2 ²	C ₂	GRY/BLK	L	11
	G ₀	G ₁	2 ⁰	2 ¹	D ₂	GRY/BRN	M	12
LSB ₁₃		G ₀		2 ⁰	A ₃	GRY/RED	N	13
OV (CIRCUIT COMMON) ¹					B ₃	GRY/ORN	P	
DIRECTION OF COUNT						ORN	R	18
CASE GROUND						GRN	S	16
0 V (CIRCUIT COMMON)						BLK	T	15
LATCH CONTROL						YEL	U	17
+V (SUPPLY VOLTAGE)						RED	V	14
SHIELD DRAIN						BARE	—	

¹Pin P is available for a tri-state option

Output Applicability Table								
	12 BITS PARALLEL	13 BITS PARALLEL	14/15 BITS	12x12 BITS	S3 SSI	S1 RS422	A1 4-20mA	A2 0-10 V
H25	•	•			•	•	•	•
H25X			•		•			
HS35	•				•		•	•
H38	•	•		•	•	•	•	•
H40	•	•		•	•	•	•	•
HMT25				•	•		•	•

Direction of Count: Standard is CW increasing when viewed from the shaft end. Pin R is normally HI (or N/C) and is pulled up internally to +V. To reverse the count direction, Pin R must be pulled LO (COMMON).

Latch control: Encoder outputs are active and provide continuous parallel position information when Pin U is HI (or N/C). Pin U is pulled up internally to +V. When Pin U is LO (COMMON) the encoder outputs are latched at the logic state that is present when the latch is applied and will stay latched until Pin U is no longer grounded.

Parallel Code (14 & 15 Bit) ²					
	Gray Code		Natural Binary		M14/19 Connector
	14 BIT	15 Bit	14 BIT	15 Bit	
MSB	G ₁₃	G ₁₄	2 ¹³	2 ¹⁴	A
	G ₁₂	G ₁₃	2 ¹²	2 ¹³	B
	G ₁₁	G ₁₂	2 ¹¹	2 ¹²	C
	G ₁₀	G ₁₁	2 ¹⁰	2 ¹¹	D
	G ₉	G ₁₀	2 ⁹	2 ¹⁰	E
	G ₈	G ₉	2 ⁸	2 ⁹	F
	G ₇	G ₈	2 ⁷	2 ⁸	G
	G ₆	G ₇	2 ⁶	2 ⁷	H
	G ₅	G ₆	2 ⁵	2 ⁶	J
	G ₄	G ₅	2 ⁴	2 ⁵	K
	G ₃	G ₄	2 ³	2 ⁴	L
	G ₂	G ₃	2 ²	2 ³	M
	G ₁	G ₂	2 ¹	2 ²	N
	LSB14	G ₀	G ₁	2 ⁰	2 ¹
LSB15	DIR CONTROL	G ₀	DIR CONTROL	2 ⁰	R
CASE GROUND					S
OV (CIRCUIT COMMON)					T
LATCH	DIR/LATCH	LATCH	DIR/LATCH		U
+V (SUPPLY VOLTAGE)	+V (SUPPLY VOLTAGE)	+V (SUPPLY VOLTAGE)	+V (SUPPLY VOLTAGE)		V

²Units Manufactured before April 2007 are LSB Justified.

SSI Output Termination Table					
	M18 CONN	M14/19 CONN	CABLE CONN	TERM. BOARD	
				H38	H40
DATA +	A	A	YEL	4	1
DATA-	H	B	WHT/YEL	7	7
CLOCK+	B	C	BLU	5	2
CLOCK-	I	D	WHT/BLU	8	8
DIR CONTROL	C	R	ORN	6	3
CASE GROUND	G	S	GRN	1	6
CIRCUIT COMMON	F	T	BLK	2	5
+V SUPPLY VOLTAGE	D	V	RED	3	4
SHIELD DRAIN	—	—	BARE	—	—

Dir/Latch on 15-Bit Encoders: Due to a limited number of connector pins, either direction of count or latch is available on pin U.

M18 Connector is a MS3102R18-1P, 10-pin connector on the encoder body and mates to an MS3106F18-1S connector or can be used with a standard cable/connector assembly, BEI P/N 924-31186-18XX (Where XX = 10, 20 30 or 50 for a 10, 20, 30, or 50 foot length). This is the preferred connector for SSI output.

M14/19 Connector is a MS3112E14-19P, 19-pin connector on the encoder body and mates to an MS3116J14-19S or equivalent.